METHOD FOR FABRICATING FLASH MEMORY DEVICE AND STRUCTURE THEREOF

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATION

[Para 1] This application claims the priority benefit of Taiwan application serial no. 92132993, filed November 25, 2003.

BACKGROUND OF THE INVENTION

[Para 2] Field of Invention

[Para 3] The present invention relates to a method for fabricating a flash memory device and a structure thereof. More particularly, the present invention relates to a method for fabricating a flash memory device having a floating gate including a plurality of nanocrystals and a structure thereof.

[Para 4] Description of Related Art

[Para 5] Since data can be written, read and erased in flash memory device many times and the data saved in the flash memory device can be kept when the power is off. Therefore, the flash memory device has become a kind of non-volatile memory device widely used in personal computer (PC) and other electronic products.

[Para 6] Typically, the floating gate and the control gate (stacked gate structure) of the flash memory device is made of doped polysilicon, wherein the floating gate and the control gate are separated by an inter-gate dielectric layer, and the floating gate and the substrate are separated by a tunneling oxide layer.

[Para 7] When data is written in the flash memory device, a bias is applied between the control gate and the source/drain region so that electrons can be injected into the floating gate. When data is read from the flash memory device by applying an operating voltage to the control gate, a channel layer underneath is then turned on/off by the charged/uncharged-floating gate and a logical value "0" or "1" is obtained, respectively. When data is erased from the flash memory device, the electric potential of a substrate, the source region, the drain region or the control gate may be raised higher than that of the floating gate. In this manner, electrons may tunnel over a tunneling oxide from the floating gate to the substrate, the source region, the drain region (i.e. substrate erase or source or drain erase) or the control gate by tunneling effect. Therefore, data writing, reading or erasing of the flash memory device is related to the quality of the floating gate.

[Para 8] However, during the manufacturing process of the flash memory device, imperfections of process may result in local impaired region in the floating gate so that the impaired memory cell can not function normally. In other words, the local impaired region resulted from manufacturing process will influence the charge storage or the charge transmission characteristic in the floating gate. Therefore, during writing, reading or erasing of the flash memory device, the impaired memory cells thereof can not normally operate.

[Para 9] In another aspect, the local impaired region of the floating gate results in the failure of the memory cells and higher manufacturing cost. In addition, the floating gate may be impaired by factors other than the process imperfections. In other words, in order to improve the yield of the flash memory device, more operation conditions are necessary in manufacturing process or other related aspects. However, it is still an issue whether or not the costs invested in the processes can be balanced off by the profits of products.

SUMMARY OF THE INVENTION

[Para 10] The invention provides a method for fabricating flash memory device and a structure thereof so as to resolve the failure issue of memory cells resulted from the local impaired region of the floating gate therein.

[Para 11] As embodied and broadly described herein, the invention provides a method for fabricating a flash memory device. The method comprises forming a tunneling oxide layer over a substrate. A floating gate having a plurality of nanocrystals and an inter-gate dielectric layer are formed over the tunneling oxide layer, wherein the material of the floating gate includes, for example, Si_XGe_{1-X} or metal silicide. A control gate is formed over the inter-gate dielectric layer, wherein a stacked gate structure includes the tunneling oxide layer, the floating gate, the inter-gate dielectric layer and the control gate. Then, a source/drain region is formed in the substrate at each side of the stacked gate structure.

[Para 12] As embodied and broadly described herein, the invention provides a structure of flash memory device comprising a substrate, a tunneling oxide layer, a floating gate, and an inter-gate dielectric layer. The tunneling oxide layer is disposed over the substrate. The floating gate is disposed over the tunneling oxide layer. The floating gate includes a plurality of nanocrystals. The material of the floating gate includes, for example, Si_XGe_{1-X} or metal silicide. The inter-gate dielectric layer covers over the nanocrystals and keeps the nanocrystals within the floating gate. The structure of flash memory device further comprises a control gate and a source/drain region. The control gate is disposed over the inter-gate dielectric layer. Also, the tunneling oxide layer, the floating gate, the inter-gate dielectric layer, and the control gate form a stacked gate structure. Furthermore, the source/drain region is formed in the substrate at each side of the stacked gate structure.

[Para 13] When the local region of the floating gate is impaired, only few of the crystals are impaired because the floating gate of the present invention includes the nanocrystals. Therefore, the charge storage or the charge transmission characteristic in the floating gate is not effectively affected, and thereby the failure issue of memory cells can be resolved.

[Para 14] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 15] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[Para 16] FIG. 1A to FIG. 1D schematically show a method for manufacturing the flash memory device of a preferred embodiment according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[Para 17] FIG. 1A to FIG. 1D schematically show a method for manufacturing the flash memory device of a preferred embodiment according to the present invention.

[Para 18] Referring to FIG. 1A, the method for manufacturing the flash memory device of the present invention comprises forming a tunneling oxide material layer 102 over a substrate 100. The material of the tunneling oxide material layer 102 includes, for example, silicon oxide, and the tunneling oxide material layer 102 may be formed by performing a thermal oxidation process. In an embodiment of the present invention, the thickness of the tunneling oxide material layer 102, for example, is about between 3.5 nm and 5.5 nm.

[Para 19] Referring to FIG. 1A, a charge storage layer 104 is then formed over the tunneling oxide material layer 102. The charge storage layer 104 may be formed by performing a low pressure chemical vapor deposition (LPCVD) process. In one embodiment of the present invention, the material of the

charge storage layer 104 includes, for example, Si_XGe_{1-X}. In another embodiment of the present invention, the material of the charge storage layer 104 includes, for example, metal silicide, such as tungsten silicide, titanium silicide, cobalt silicide or nickel silicide. Take tungsten silicide (W_YSi_Z) as an example, the value of Y is about between 0.5 and 5, and the value of Z is about between 1 and 3.

[Para 20] In addition, according to various materials of the charge storage layer 104, the process parameters adopted for LPCVD process may be different. For example, in an embodiment of the present invention, when the material of the charge storage layer 104 is Si_XGe_{1-X}, a reactive gas adopted for LPCVD process includes, for example, SiH_4 or GeH_4, an operating pressure, for example, is about between 1 and 1000 mTorrs, and a process temperature, for example, is about between 600 and 800 degrees centigrade.

[Para 21] Furthermore, in another embodiment of the present invention, when the material of the charge storage layer 104 is tungsten silicide, a reactive gas adopted for LPCVD process includes, for example, WF_6, SiH_4, Si_2H_6 or SiH_2Cl_2, an operating pressure, for example, is about between 1 and 1000 mTorrs, and a process temperature, for example, is about between 300 and 800 degrees centigrade.

[Para 22] Referring to FIG. 1B, a thermal oxidation process is then performed, and a portion of the charge storage layer 104 is oxidized to form an inter-gate dielectric material layer 106, such as silicon germanium oxide layer or metal silicon oxide layer. While, other portion of the charge storage layer 104 not being oxidized is converted into a plurality of nanocrystals. The nanocrystals mentioned above form a floating gate material layer 108. In an embodiment of the present invention, the thermal oxidation process, for example, is a rapid thermal oxidation process. During the rapid thermal oxidation process, gases including oxygen, such as O_2, H_2O or NO_x, are provided. Furthermore, a process temperature of the rapid thermal oxidation process is about between 850 and 1000 degrees centigrade, and a more preferred process temperature is about 950 degrees centigrade.

[Para 23] It is noted that when the local region of the floating gate material layer 108 is impaired, only few of the crystals is impaired. Since the floating gate material layer 108 of the present invention includes the nanocrystals mentioned above, the floating gate material layer 108 can function normally via the region without impaired nanocrystals. Therefore, the charge storage or the charge transmission characteristic in the floating gate material layer 108 is not influenced.

[Para 24] Referring to FIG. 1C, a control gate material layer 110 is then formed over the inter-gate dielectric material layer 106. The material of the control gate material layer 110 includes, for example, doped polysilicon. The doped polysilicon may be formed by depositing an un-doped polysilicon layer, and then performing an ion implantation process. In addition, the control gate material layer 110 may be formed by performing an in-situ CVD process with reactive gases including dopants.

[Para 25] Referring to FIG. 1D, the tunneling oxide material layer 102, the floating gate material layer 108, the inter-gate dielectric material layer 106 and the control gate material layer 110 are then patterned to form a tunneling oxide layer 102a, a floating gate 108a, an inter-gate dielectric layer 106a and a control gate 110a, respectively. The tunneling oxide layer 102a, the floating gate 108a, the inter-gate dielectric layer 106a and the control gate 110a form a stacked gate structure 112. The method of patterning, for example, is a conventional photolithography/etch process.

[Para 26] Referring FIG. 1D, the manufacturing process is carried out by forming a source region 114a and a drain region 114b in the substrate 100 at each side of the stacked gate structure 112. The source region 114a and the drain region 114b, for example, is formed by performing a conventional ion implantation process with the stacked gate structure 112 as an implantation mask.

[Para 27] The detail structure of the flash memory device of the present invention will be described as follow. Referring to FIG. 1D, a memory cell of the flash memory device comprises the substrate 100, the tunneling oxide layer 102a, the floating gate 108a, the inter-gate dielectric layer 106a, the

control gate 110a, the source region 114a and the drain region 114b. In the structure of FIG. 1D, the floating gate 108a includes a plurality of nanocrystals. The stacked gate structure 112 includes the tunneling oxide layer 102a, the floating gate 108a, the inter-gate dielectric layer 106a and the control gate 110a.

[Para 28] Furthermore, the tunneling oxide layer 102a is disposed over the substrate 100. The material of the tunneling oxide layer 102a includes, for example, silicon oxide.

[Para 29] The floating gate 108a is disposed over the tunneling oxide layer 102a, and the material of the floating gate 108a includes, for example, Si_XGe_{1-X} or metal silicide. In another embodiment of the present invention, the material of the floating gate 108a includes, for example, metal silicide, such as tungsten silicide, titanium silicide, cobalt silicide or nickel silicide. When the material of the floating gate 108a is tungsten silicide (W_YSi_Z), the value of Y is about between 0.5 and 5, and the value of Z is about between 1 and 3.

[Para 30] The inter-gate dielectric layer 106a covers the nanocrystals (the floating gate 108a) and keeps the nanocrystals within the floating gate 108a. The material of the inter-gate dielectric layer 106a includes, for example, an oxide of the material of the floating gate 108a.

[Para 31] The structure of flash memory device further comprises a control gate 110a and a source/drain region 114a/114b. The control gate 110a is disposed over the inter-gate dielectric layer 106a, and a stacked gate structure 112 includes the tunneling oxide layer 102a, the floating gate 108a, the inter-gate dielectric layer 106a and the control gate 110a. Furthermore, the source/drain region 114a/114b is formed in the substrate 100 at each side of the stacked gate structure 112. When the material of the floating gate 108a is Si_XGe_{1-X}, the material of the inter-gate dielectric layer 106a is silicon germanium oxide. When the material of the floating gate 108a is metal silicide, the material of the inter-gate dielectric layer 106a is metal silicon oxide.

[Para 32] In addition, the control gate 110a is disposed over the inter-gate dielectric layer 106a. The material of the control gate 110a includes, for example, doped polysilicon.

[Para 33] Furthermore, the source region 114a and the drain region 114b are formed in the substrate 100 at each side of the stacked gate structure 112.

[Para 34] As described above, the present invention at least comprises advantages as follow.

[Para 35] 1. When the local region of the floating gate is impaired, only few of the crystals are impaired because the floating gate of the present invention includes the nanocrystals. Therefore, the charge storage or the charge transmission characteristic in the floating gate is not influenced, and thereby the failure issue of memory cells can be resolved.

[Para 36] 2. In the flash memory device of the present invention, the nanocrystals in the floating gate can make hysteresis effect obvious, and thereby the ability of charge storage can be enhanced.

[Para 37] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention if they fall within the scope of the following claims and their equivalents.